CLOCK AND DATA RECOVERY CIRCUIT AND METHOD

ABSTRACT OF THE DISCLOSURE

In a clock and data recovery circuit and method, the clock and data recovery circuit comprises a clock signal generator for generating N clock signals, each clock signal having phase difference of 360/N x K from each other, wherein the N denotes an integer and the K denotes an integer from 0 to N-1, a phase selector for generating an $I+2_{th}$ clock signal out of the N clock signals as a recovered clock signal if an I_{th} clock signal is on a first state and an $I+1_{th}$ clock signal is on a second state when logic level transition of a received data is detected, wherein the I denotes an integer from 1 to N, and a recovered data generator for generating a recovered data synchronized with the recovered clock signal by using the received data in response to the recovered clock signal output from the phase selector.

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